CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a semiconductor structure, said method comprising the steps of:

forming at least one isolation region within said semiconductor substrate; and

forming a plurality of gate stacks over said semiconductor substrate, at least two of said plurality of gate stacks being in contact with said isolation region and being spaced apart from each other by less than 400 Angstroms.

2. The method of claim 1, wherein said act of forming said plurality of gate stacks further comprises forming a plurality of gate layers over said substrate and said isolation region, and an insulating layer over said plurality of gate layers.

3. The method of claim 2, wherein said act of forming said plurality of gate stacks further comprises defining a first opening through a first photoresist layer formed over said insulating layer, said first opening being located over said isolation region.

4. The method of claim 3, wherein said act of forming said plurality of gate stacks further comprises defining a second opening within said insulating layer, said second opening being in communication with said first opening.

5. The method of claim 4, wherein said act defining said second opening further comprises taper etching said insulating layer using said first photoresist layer as a mask.

6. The method of claim 4, wherein said second opening has a tapered profile.

7. The method of claim 4, wherein said act of forming said plurality of gate stacks further comprises defining a first trench through said gate layers, said first trench being in communication with said second opening and said isolation region.

8. The method of claim 7, wherein said act of forming said plurality of gate stacks further comprises etching said gate layers selective to said insulating layer to obtain said first trench.

9. The method of claim 8, wherein said first trench has a width of about 100 Angstroms to about 400 Angstroms.

10. The method of claim 8, wherein said first trench has a width of about 100 Angstroms to about 200 Angstroms.

11. The method of claim 8, wherein said act of forming said plurality of gate stacks further comprises locating a first filler material in said first trench and said second opening to form a first filler plug, said first filler plug being in contact with said isolation region.

12. The method of claim 11, wherein said first filler material is formed of a material selected from the group consisting of oxides and nitrides.

13. The method of claim 12, wherein said first filler material and said insulating layer are formed of same material.

14. The method of claim 11, wherein said act of forming said plurality of gate stacks further comprises forming a second photoresist layer over said insulating layer and said first filler plug.

15. The method of claim 14, wherein said act of forming said plurality of gate stacks further comprises patterning said gate layers lateral to said first filler plug and said isolation region.

16. The method of claim 15, wherein said act of forming said plurality of gate stacks further comprises removing said insulating material and said first filler plug to obtain said gate stacks.

17. The method of claim 3, wherein said act of forming said plurality of gate stacks further comprises defining a third opening within said insulating layer, said third opening having a width similar to that of the first opening.

18. The method of claim 17, wherein said act of forming said plurality of gate stacks further comprises reducing said width of said third opening by forming a plurality of spacers on sidewalls of said third opening.

19. The method of claim 18, wherein said act of forming said plurality of gate stacks further comprises defining a second trench through said gate layers, said second trench being in communication with said third opening and said isolation region.

20. The method of claim 19, wherein said act of forming said plurality of gate stacks further comprises etching said gate layers selective to said spacers to obtain said second trench.

21. The method of claim 20, wherein said second trench has a width of about 100 Angstroms to about 400 Angstroms.

22. The method of claim 20, wherein said second trench has a width of about 100 Angstroms to about 200 Angstroms.

23. The method of claim 20, wherein said act of forming said plurality of gate stacks further comprises locating a second filler material in said second trench and said second opening to form a second filler plug, said second filler plug being in contact with said isolation region.

24. The method of claim 23, wherein said second filler material is formed of a material selected from the group consisting of oxides and nitrides.

25. The method of claim 24, wherein said second filler material and said insulating layer are formed of same material.

26. The method of claim 23, wherein said act of forming said plurality of gate stacks further comprises forming a third photoresist layer over said insulating layer and said second filler plug.

27. The method of claim 26, wherein said act of forming said plurality of gate stacks further comprises patterning said gate layers lateral to said second filler plug and said isolation region.

28. The method of claim 27, wherein said act of forming said plurality of gate stacks further comprises removing said insulating material and said second filler plug to obtain said gate stacks.

29. The method of claim 1, wherein said structure is part of a memory device.

30. The method of claim 29, wherein said gate stacks form word lines of said memory device.

31. The method of claim 30, wherein said memory device is a DRAM memory device.

32. The method of claim 1, wherein said structure is part of a memory circuit coupled to a processor, wherein at least one of said processor and said memory circuit contains said plurality of gate stacks.

33. The method of claim 1 further comprising the act of forming a source/drain region in said semiconductor substrate disposed adjacent to said plurality of gate stacks and lateral to said isolation region.

34. The method of claim 33 further comprising the act of forming a capacitor over said source/drain region.

35. A method of forming a plurality of gate stacks over a substrate, said method comprising forming at least two adjacent gate stacks over said substrate, said adjacent gate stacks being spaced apart from each other by less than 400 Angstroms.

36. The method of claim 35, wherein said act of forming said gate stacks further comprises forming a plurality of gate layers over said substrate including an isolation region, and forming an insulating layer over said gate layers.

37. The method of claim 36, wherein said act of forming said gate stacks further comprises forming a first photoresist layer over said insulating layer.

38. The method of claim 37, wherein said act of forming said gate stacks further comprises forming a first opening through said first photoresist layer, and etching said insulating layer to define a second opening through said insulating layer, said second opening being in communication with said first opening.

39. The method of claim 38, wherein said second opening has a tapered profile.

40. The method of claim 39, wherein said act of forming said gate stacks further comprises forming a trench through said gate layers, said trench being in communication with said second opening and said isolation region.

41. The method of claim 40, wherein said act of forming said gate stacks further comprises etching said gate layers selective to said insulating layer to obtain said trench.

42. The method of claim 41, wherein said trench has a width of about 100 Angstroms to about 400 Angstroms.

43. The method of claim 41, wherein said trench has a width of about 100 Angstroms to about 200 Angstroms.

44. The method of claim 41, wherein said act of forming said gate stacks further comprises locating a filler material in said trench and said second opening to form a filler plug, said filler plug being in contact with said isolation region.

45. The method of claim 44, wherein said act of forming said gate stacks further comprises forming a second photoresist layer over said insulating layer and said filler plug.

46. The method of claim 45, wherein said act of forming said gate stacks further comprises patterning said gate layers lateral to said filler plug and said isolation region.

47. The method of claim 46, wherein said act of forming said gate stacks further comprises removing said insulating material and said filler plug to obtain said gate stacks.

48. The method of claim 44, wherein said insulating layer and said filler plug are formed of a similar material.

49. The method of claim 35, wherein said gate stacks form word lines of a memory device.

50. A method of forming gate stacks over a substrate, said method comprising forming at least two adjacent gate stacks over an isolation region of said substrate, said adjacent gate stacks being spaced apart from each other by less than 400 Angstroms.

51. The method of claim 50, wherein said act of forming said gate stacks further comprises forming a plurality of gate layers over said substrate including said isolation region, and forming an insulating layer over said gate layers.

52. The method of claim 51, wherein said act of forming said gate stacks further comprises forming an opening through said insulating layer.

53. The method of claim 52, wherein said act of forming said gate stacks further comprises reducing said width of said opening by forming a plurality of spacers on sidewalls of said opening.

54. The method of claim 53, wherein said act of forming said gate stacks further comprises defining a trench through said gate layers, said trench being in communication with said opening and said isolation region.

55. The method of claim 54, wherein said act of forming said gate stacks further comprises etching said gate layers selective to said plurality of spacers to obtain said trench.

56. The method of claim 55, wherein said trench has a width of about 100 Angstroms to about 400 Angstroms.

57. The method of claim 55, wherein said trench has a width of about 100 Angstroms to about 200 Angstroms.

58. The method of claim 55, wherein said act of forming said gate stacks further comprises locating a filler material in said trench and said opening to form a filler plug, said filler plug being in contact with said isolation region.

59. The method of claim 58, wherein said act of forming said gate stacks further comprises forming a photoresist layer over said insulating layer and said filler plug.

60. The method of claim 59, wherein said act of forming said gate stacks further comprises patterning said gate layers lateral to said filler plug and said isolation region.

61. The method of claim 60, wherein said act of forming said gate stacks further comprises removing said insulating material and said filler plug to obtain said gate stacks.

62. The method of claim 58, wherein said insulating layer and said filler plug are formed of a similar material.

63. The method of claim 50, wherein said gate stacks form word lines of a memory device.

64. The method of claim 63, wherein said memory device is a DRAM memory device.

65. A memory structure comprising:

a plurality of word lines formed over a semiconductor substrate, at least two adjacent ones of said plurality of word lines being spaced apart from each other by a distance of less than 400 Angstroms.

66. The memory structure of claim 65 further comprising a plurality of bit lines formed over and in contact with said plurality of word lines.

67. The memory structure of claim 65 further comprising an isolation region formed below said at least two adjacent ones of said plurality of word lines being spaced apart from each other by a distance of less than 400 Angstroms.

68. The memory structure of claim 65, wherein each of said plurality of word lines further comprises a plurality of gate layers.

69. The memory structure of claim 68, wherein each of said plurality of word lines includes a polysilicon layer.

70. The memory structure of claim 68, wherein each of said plurality of word lines includes a metal silicide layer.

71. The memory structure of claim 65, wherein said memory structure is a DRAM structure.

72. The memory structure of claim 65, wherein said memory structure is a SRAM structure.

73. A memory device comprising a plurality of DRAM cells, said DRAM cells including a plurality of word lines formed over a semiconductor substrate, at least two of said plurality of word lines being spaced apart from each

other by a distance less than about 400 Angstroms, and a plurality of bit lines formed over said plurality of word lines.

74. The memory device of claim 73 further comprising an isolation region formed below and in contact with said at least two of said plurality of word lines being spaced apart from each other by a distance less than about 400 Angstroms.